Journal of Low Temperature Physics manuscript No.
(will be inserted by the editor)

T. Wada[1] · **H. Nagata**[1] · **H. Ikeda**[1] · **Y. Arai**[2] · **M. Ohno**[3] **and K. Nagase**[1,4]

Development of low power cryogenic readout integrated circuits using fully-depleted-silicon-on-insulator CMOS technology for far-infrared image sensors

17.07.2011

Keywords low temperature, low power, FD-SOI CMOS, readout IC, infrared astronomy

Abstract We are developing low power cryogenic readout integrated circuits (ROICs) for large format far-infrared image sensors using fully-depleted-silicon-on-insulator (FD-SOI) CMOS technology. We have evaluated the characteristics of MOS FETs fabricated by the FD-SOI CMOS technology and have found that both p-ch and n-ch FETs show good static performance below the liquid helium temperature, where n-ch FETs fabricated by conventional bulk-CMOS technology usually suffer from anomalous behaviors such as kink and hysteresis. We have also designed and fabricated an operational amplifier (OP-AMP) and have successfully demonstrated that the OP-AMP works at the liquid helium temperature with an open loop gain of 7000, a noise of $19\mu W/\sqrt{Hz}$ at 1 Hz, and a power consumption of 1.3 μW.

PACS numbers: 74.70.Tx,74.25.Ha,75.20.Hr

1 Introduction

Recent successes of Spitzer/MIPS[1], AKARI/FIS[2], and Herschel/PACS[3] clearly demonstrated the power of large format imaging sensors in the far-infrared (FIR) astronomy both for imaging and spectroscopic observations. In these space borne far-infrared observatories, germanium FIR detectors and silicon MOSFET read

1:Institute of Space and Astronautical Science, Japan Aerospace Exploration Agency, Sagamihara, Kanagawa 252-5210, Japan
Tel.:+81-50-336-22748
Fax:+81-42-786-7202
E-mail: wada@ir.isas.jaxa.jp
2: High Energy Accelerator Research Organization, Tsukuba, Ibaraki 305-0801, Japan
3: National Institute of Advanced Industrial Science and Technology, Tsukuba, Ibaraki 305-8568, Japan
4: The Graduate University for Advanced Studies, Sagamihara, Kanagawa 252-5210, Japan

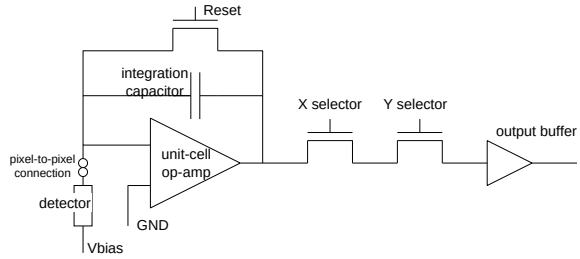

Fig. 1 Typical system diagram of ROIC for far-infrared imaging sensors.

out integrated circuits (ROIC) were employed. Figure 1 shows a typical system diagram of ROIC for far-infrared imaging sensors. The detectors and the ROICs were cooled down to cryogenic temperatures (below 4K) in order to reduce the thermal dark current. Because the performance of bulk CMOSs is often degraded due to carrier freeze-out effect at the cryogenic temperatures, large amount of effort is made such as special semiconductor process for cryogenic temperature[4], novel FET structure using BiCMOS[5] and special circuit technique[6].

However, the performance of these ROIC is not high enough for the next generation FIR space telescope, such as SPICA[7]. Unlike the previous FIR astronomical missions, SPICA does not need any cryogen (no liquid helium), and is cooled by radiative cooling and mechanical coolers[8]. This architecture results in reduction of mass for vacuum chamber, a larger aperture telescope, longer mission life time, but smaller cooling power at the focal plain instruments (5mW at 1.7K stage in case of SPICA). Consequently, the ROICs has to be operated at cryogenic temperature with less than a few mW power consumptions, a few μW per pixel for a 32x32 class imaging sensor; a factor of ten reduction in power consumptions is necessary. In addition, lower leak current (higher off-resistance) is also required for the ROICs because the next generation FIR detectors, such as germanium BIB detectors[9], has lower dark current compare to conventional germanium photoconductors.

Recently, we have found that a fully-depleted silicon on insulator (FD-SOI) CMOS, which is produced by OKI-semiconductor co. ltd.[10], shows an excellent cryogenic performance if it is fabricated with source tie (ST) or body tie (BT) structure[11]. Because the ST FD-SOI FETs show excellent cryogenic performance both for n-channel and p-channel, we can take advantage of well established standard CMOS circuit technologies. Using this process, we have fabricated two chips, one which contains basic analog circuits including operational amplifiers (OP-AMP) and an off-resistance evaluation circuit in 2008, and one which contains basic analog-digital circuits including analog-to-digital converter and digital-to-analog converter in 2009[12], in order to verify the capability of the FD-SOI-CMOS for the ROIC of the far-infrared imaging sensors.

In this paper, we describe the performance of the FD-SOI CMOS FETs and the OP-AMP including off-resistance of the switch circuit at cryogenic temperature.

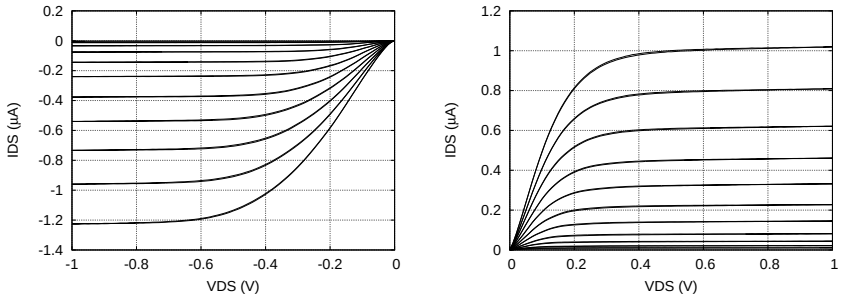

Fig. 2 I-V curves of the FD-SOI PMOS (left) and NMOS (right) at 4K.

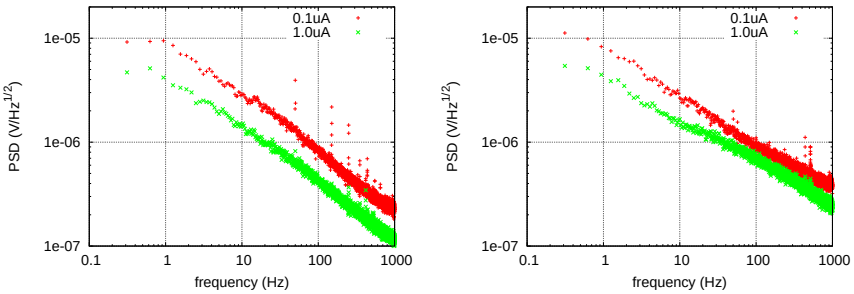

Fig. 3 (Color online) Input referred noise spectra of the FD-SOI PMOS (left) and NMOS (right) at 4K.

2 Experimental results

The I-V curves and the noise spectra of the FD-SOI MOSFETs at 4K are shown in figures 2 and 3. In order to check the repeatability in fabrications, we have fabricated the same FETs (source tie, W/L=0.63μm/5μm) as the previous fabrication. No strong kink nor hysteresis is found in the I-V curves both for p-channel and n-channel FETs as the previous fabrication. The noise spectra are also similar. The result of characterization at 4K is summarized in table 1.

Figure 4 shows the schematic diagram of the OP-AMP. We have used source tie FETs with gate size of W/L=0.63μm/5μm except the input FETs (W/L=5μm/5μm). The result of characterization at 4K is summarized in table 2. The detail of the measurement is described in the other paper[12].

In order to measure the leak current at the level of $10^{-16}A$, we have fabricated a test circuit (figure 5). After charging up the capacitor, we monitor the output voltage decreasing by the leak current at the switch FET. The leak current is measured to be 1.2×10^{-16} A from the voltage trend at 150-240 second corresponding to the off-resistance of $7.5 \times 10^{15} \Omega$ taking into account of shift in applied voltage from 1.0V to 0.9V at switching-off by the feed through.

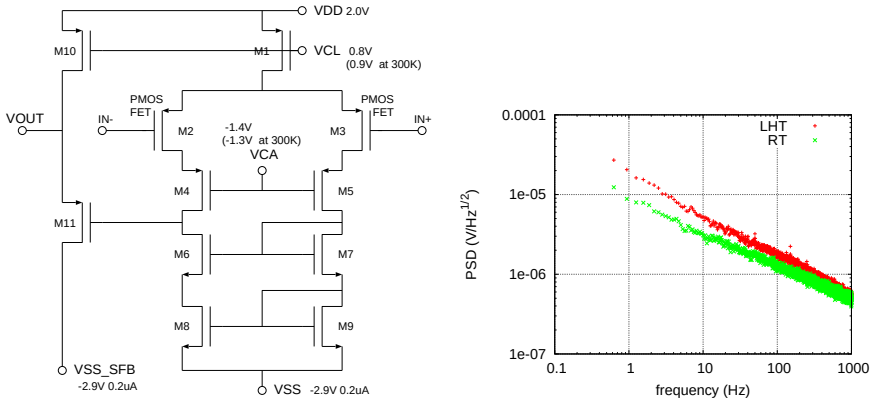

Fig. 4 (Color online) Schematic diagram of the OP-AMP (left). All FETs are ST FD-SOI-CMOS with a gate size of W/L=0.63/5.0, except the input PMOSs (W/L=5/5). Input referred noise spectra (right) of the OP-AMP at liquid helium temperature (LHT) and room temperature (RT).

Table 1 Characteristics of FD-CMOS FETs at 4K

	$g_m^\dagger$ μS	$r_d^\dagger$ MΩ	noise† at 1 Hz $\mu V/\sqrt{Hz}$	off-resistance‡ Ω
PMOS*	1.8	$>$100	10	–
NMOS*	3.0	$>$100	7	$> 7.5 \times 10^{15}$

$*$: W/L=0.63μm/5.0μm ST-FD-SOI, LVT
$\dagger$: VDS=1V, IDS=0.1μA
$\ddagger$: W/L=5μm/10μm, VDS=0.9V

Table 2 Characteristics of FD-CMOS OP-AMP at 4K

	design	measurement	
temperature	4K	4–300K$*$	excellent
open loop gain	$>$ 1000	7000	excellent
Output swing	$> 1V$	1.3V	excellent
input referred noise	14-20$\mu V/\sqrt{Hz}$	19$\mu V/\sqrt{Hz}$	good
power	1.1μW	1.3μW	good
input offset	0mV	2mV	good

$*$: adjustment of bias voltage is required in room temperature operation.

3 Discussions

In case of the next generation space FIR telescope with the next generation FIR detector, the thermal radiation from the telescope and the dark current of the detector should be less than the natural background which consists of zodiacal light, galactic cirrus emission and the cosmic infrared background. In order to achieve background limited observations, the ROIC must has less leak current compared with the photo-current and less noise compared with the shot noise of the the photo-current produced by the natural background in each pixel.

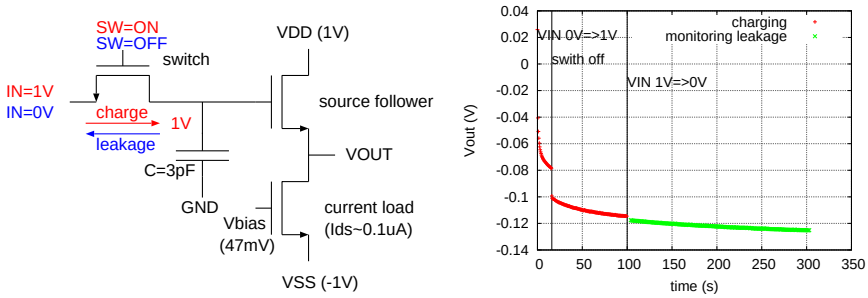

Fig. 5 (Color online) Test circuit for leak current measurement (left) and the output trend (right). The capacitor (3pF) is first charged up to the input level (1V) by switch-on. After switch-off, the input level is shifted to 0V. The leak current of the switch FET shifts the voltage at the capacitor node. The shift of the voltage is observed through the source follower. The source follower gain is 0.94±0.01. The leak current and off-resistance is estimated to be 1.2×10^{-16} A and $7.5 \times 10^{15} \Omega$ from the voltage trend at 150-240 second.

Table 3 Background signal for a cryogenic space telescope with Nyquist sampling pixel scale

wavelength μm	sky brightness* MJy/str	sky signal† e/s/pixel	pixel scale‡ arcsec
2.2	0.11	2.4e-02	0.076
25	18	5.0e+02	0.86
100	2.5	1.1e+03	3.4
240	1.8	4.6e+03	8.2

∗: DIRBE/COBE dark sky[13]
†: adopting a spectral resolution $R = 10$ and a total efficiency $\eta = 0.15$
‡: a pixel scale at each wavelength band for a telescope diameter of 3.0m

The number of the background photons in each pixel in unit time can be calculated as follows.

$$N_{\lambda,BG,pix} = I_{\nu,BG} \frac{c}{\lambda^2} \Omega_{pix} A_{tel} \frac{1}{E_{photon}} \eta d\lambda = I_{\nu,BG} \frac{\lambda^4}{16} \frac{\pi}{hc} \frac{\eta}{R}, \quad (1)$$

where $I_{\nu,BG}$ is the sky brightness, Ω_{pix} is the solid angle of a pixel, $d\lambda = \lambda/R$ is the band width at the spectral resolution of R, $A_{tel} = \pi(D/2)^2$ is the effective area of the telescope (diameter of D), $E_{photon} = hc/\lambda$ is the photon energy, and η is the total quantum efficiency including the optics and the detector. The solid angle of a pixel can be written as $\Omega_{pix} = (\lambda/2D)^2$ if the pixel samples the telescope's point spread function (PSF) in proper Nyquist condition. Table 3 shows the number of the natural background signal in unit of electron per pixel per unit time adopting the measurement of the natural background by DIRBE/COBE[13], the spectral resolution $R = 10$, and the optical/detector efficiently $\eta = 0.15$.

In the FIR wavelength regions, order of 1000 electron/sec natural background signal is expected. The leak current of the ROIC must be less than 1000 e/s and the measured leak current of the switch FET is mostly acceptable. The ROIC must also has less noise compared with the shot noise produced by the natural

background ($\sqrt{1000} \sim 30$ electron in 1 second exposure per pixel). Adopting the integration capacitance (figure 1) of $C = 0.1pF$, this corresponds to $48\mu V$. With the input referred noise of the OP-AMP ($19\mu V/\sqrt{Hz}$), it is possible to keep the system noise less than this value if we choose appropriate exposure time.

Dynamic range is also important because the standard star in the far-infrared astronomy is quite bright (a few Jy, Jy=$1.0^{-26}W/m^2/Hz$) compared with the faint target (a few μ Jy) of the next generation FIR space observatories (such as high-redshift primeval galaxies). The output swing (1.3V) and input referred noise ($19\mu V/\sqrt{Hz}$) give an order of 10^5 in dynamic range and this is sufficient if we use appropriate secondary standard stars.

Input offset voltage (2mV) is negligible compared with bias voltage of Ge:Ga FIR photo-conductor (or BIB detector). However, the variation of the offset voltage may affect the uniformity of photo-response among the pixels in case of direct hybrid sensors[14], in which the ROIC has pixel-to-pixel connecttion to a monolithic detector array. Further investigation of the variation is required.

The power (1.3μW/pixel) is acceptable for the next generation 32x32 pixels class FIR imaging sensor. We may need further optimization in parameters (W/L for each MOSFETs) for a 64x64 pixel sensor.

4 Conclusions

We have investigated the cryogenic characteristics of FD-SOI CMOS FETs and OP-AMP. We have found that both p- and n-channel FET have good characteristics at the LHT if they have source tie structure. We have confirmed that the characteristics are reproduced in multiple productions. The OP-AMP also shows good characteristics at the LHT. FD-SOI-CMOS has been proven to be an appropriate process for the ROIC of the next generation far-infrared imaging sensors.

Acknowledgements This work was supported by KAKENHI (21760321,23340053,20244016).

References

1. G.H. Rieke, et al., *ApJ* **154**, 25, (2004)
2. M. Kawada, et al., *PASJ* **59**, S389, (2007)
3. A. Poglitsch, et al., *Astron. Astrophys.* **518**, L2, (2010)
4. E. Y. Young, et al., *Proc. SPIE* **3354**, 57, (1998)
5. H. Nagata, et al., *IEEE Tran. Electron.* **51**, 270, (2004)
6. P. Merken, et al., *Proc. SPIE* **6275**, 627516, (2006)
7. T. Nakagawa, *SPIE* **7731**, 77310O, (2010)
8. H. Sugita, *Cryogenics* **50**, 566, (2010)
9. H. Kaneda, et al., *JJAP* **50**, 066503, (2011)
10. A. Uchiyama, et al., *IEEE International SOI Conference Proceedings* **2006**, 15, (2006)
11. H. Nagata, et al., *AIP Conf. Proc.* **1185**, 267, (2009)
12. H. Nagata, et al., *IEICE Trans. Commun.* **E94-B**, in press, (2011)
13. M.G. Hauser, *AIP Conf. Proc.* **348**, 11, (1996)
14. M Fujiwara, et al., *Appl. Optics.* **42**, 2166, (2003)