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Development of low power cryogenic readout integrated circuits using fully-depleted-silicon-on-insulator CMOS technology for far-infrared image sensors

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Abstract We are developing low power cryogenic readout integrated circuits (ROICs) for large format far-infrared image sensors using fully-depleted-silicon-on-insulator (FD-SOI) CMOS technology. We have evaluated the characteristics of MOS FETs fabricated by the FD-SOI CMOS technology and have found that both p-ch and n-ch FETs show good static performance below the liquid helium temperature, where n-ch FETs fabricated by conventional bulk-CMOS technology usually suffer from anomalous behaviors such as kink and hysteresis. We have also designed and fabricated an operational amplifier (OP-AMP) and have successfully demonstrated that the OP-AMP works at the liquid helium temperature with an open loop gain of 7000 and a power consumption of $1.3 \mu\text{W}$. The noise is dominated by mainly $1/f$ and has a value of $19 \mu\text{V}/\sqrt{\text{Hz}}$ at 1 Hz.

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1 Introduction

Recent successes of Spitzer/MIPS¹, AKARI/FIS², and Herschel/PACS³ clearly demonstrated the power of large format imaging sensors in the far-infrared (FIR) astronomy both for imaging and spectroscopic observations. In these space borne far-infrared observatories, germanium FIR detectors and silicon MOSFET Read

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Out Integrated Circuits (ROIC) were employed. Figure 1 shows a typical system diagram of ROIC for far-infrared imaging sensors. The detectors and the ROICs were cooled down to cryogenic temperatures (below 4K) in order to reduce the thermal dark current. Because the performance of bulk CMOSs is often degraded by carrier freeze-out effect at cryogenic temperatures, large amount of effort is made such as special semiconductor process for cryogenic temperature⁴, novel FET structure using BiCMOS⁵ and special circuit technique⁶.

However, the performance of these ROIC is not high enough for the next generation FIR space telescope, such as SPICA⁷. Unlike the previous FIR astronomical missions, SPICA does not need any cryogen (no liquid helium), and is cooled by radiative cooling and mechanical coolers⁸. This architecture results in reduction of mass for vacuum chamber, a larger aperture telescope, longer mission life time, but smaller cooling power at the focal plain instruments (5 mW at 1.7 K stage in case of SPICA). Consequently, the ROICs has to be operated at cryogenic temperature with less than a few mW power consumptions, a few μW per pixel for a 32x32 class imaging sensor; a factor of ten reduction in power consumptions is necessary compared to that of AKARI/FIS ROIC⁵. In addition, lower leakage current (higher off-resistance) is also required for the ROICs because the next generation FIR detectors, such as germanium BIB detectors⁹, have lower dark current compared to conventional germanium photo-conductors.

Unlike bulk CMOS, fully-depleted silicon on insulator (FD-SOI) MOSFETs have small or no kink effect even at cryogenic temperature because of the reduction of the drain electric field (small amount of impact ionization) and the reduction of substrate-to-source potential barrier (small accumulation of holes in the substrate)¹⁰. Recently, we have found that a 0.20 μm FD-SOI CMOS, which is produced by OKI-semiconductor co. ltd.¹¹, shows an excellent cryogenic performance if it is fabricated with source tie (ST) or body tie (BT) structure¹². Because the ST FD-SOI FETs show excellent cryogenic performance both for n-channel and p-channel, we can take advantage of well established standard CMOS circuit technologies. Using this process, we have fabricated two chips, one in 2008 which contains basic analog circuits including operational amplifiers (OP-AMP) and an off-resistance evaluation circuit; another chip, developed in 2009, contains basic analog-digital circuits including analog-to-digital converter and digital-to-analog converter¹³, in order to verify the capability of the FD-SOI-CMOS for the ROIC of the far-infrared imaging sensors.

In this paper, we describe the performance of the FD-SOI CMOS FETs and the OP-AMP including off-resistance of the switch circuit at cryogenic temperature.

2 Experimental results

The I-V curves and the noise spectra of the FD-SOI MOSFETs at 4 K are shown in figures 2 and 3. In order to check the repeatability in fabrications, we have fabricated the same FETs (source tie, $W/L=0.63 \mu\text{m}/5 \mu\text{m}$) as the previous fabrication. No strong kink nor hysteresis is found in the I-V curves both for p-channel and n-channel FETs as the previous fabrication. The noise spectra are also similar. The result of characterization at 4 K is summarized in table 1.

Figure 4 shows the schematic diagram of the OP-AMP. We have used source tie FETs with gate size of $W/L=0.63 \mu\text{m}/5 \mu\text{m}$ except the input FETs ($W/L=5$

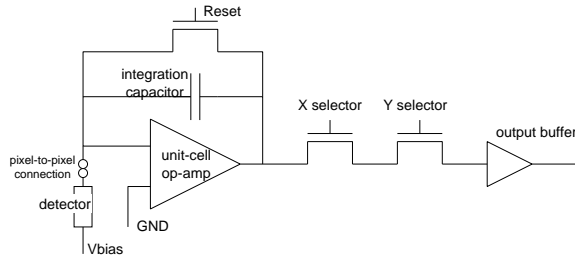


Fig. 1 Typical system diagram of ROIC for far-infrared imaging sensors.

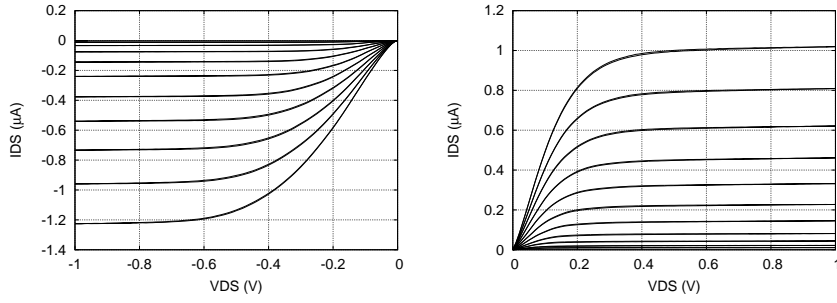


Fig. 2 I-V curves of the FD-SOI PMOS (left) and NMOS (right) at 4 K.

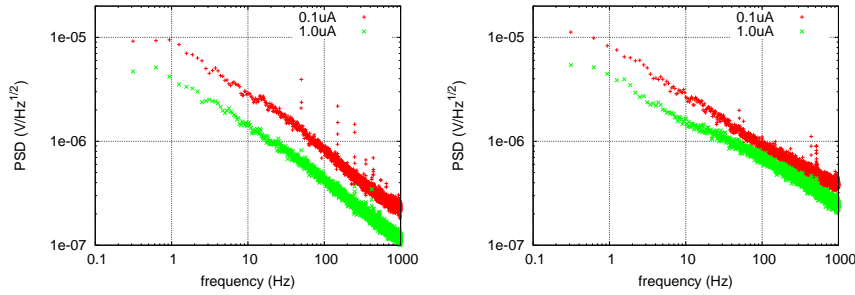


Fig. 3 (Color online) Input referred noise spectra of the FD-SOI PMOS (left) and NMOS (right) at 4 K.

$\mu\text{m}/5 \mu\text{m}$). The result of characterization at 4 K is summarized in table 2. The detail of the measurement is described in the other paper¹³.

To characterize parallel noise, we measured the leakage current of the feedback reset switch of figure 1 at the level of 10^{-16} A, by means of the dedicated test circuit shown in figure 5. After charging up the capacitor, we monitor the output voltage decreasing by the leakage current at the switch FET. The leakage current is measured to be 1.2×10^{-16} A from the voltage trend at 150-240 second corresponding to the off-resistance of $7.5 \times 10^{15} \Omega$ taking into account of shift in applied voltage from 1.0 V to 0.9 V at switching-off by the feed through.

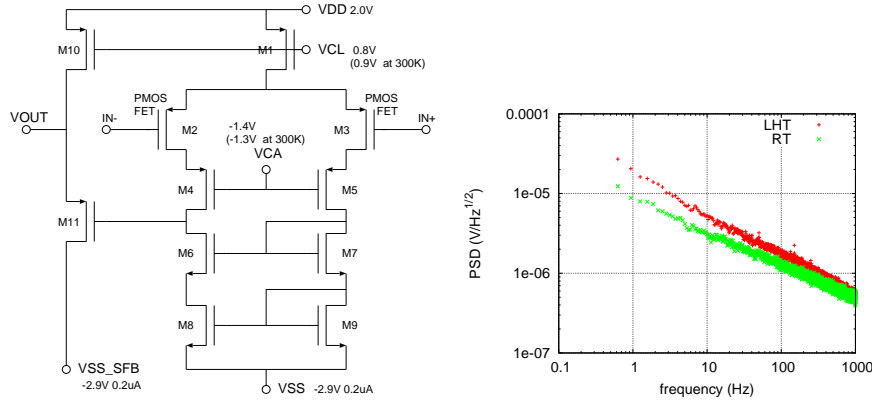


Fig. 4 (Color online) Schematic diagram of the OP-AMP (left). All FETs are ST FD-SOI-CMOS with a gate size of $W/L=0.63/5.0$, except the input PMOSs ($W/L=5/5$). Input referred noise spectra (right) of the OP-AMP at liquid helium temperature (LHT) and room temperature (RT).

Table 1 Characteristics of FD-CMOS FETs at 4 K

	g_m^\dagger μS	r_d^\ddagger $\text{M}\Omega$	noise [†] at 1 Hz $\mu\text{V}/\sqrt{\text{Hz}}$	off-resistance [‡] Ω
PMOS*	1.8	>100	10	–
NMOS*	3.0	>100	7	$> 7.5 \times 10^{15}$

*: $W/L=0.63 \mu\text{m}/5.0 \mu\text{m}$ ST-FD-SOI, LVT

†: $V_{DS}=1 \text{ V}$, $I_{DS}=0.1 \mu\text{A}$

‡: $W/L=5 \mu\text{m}/10 \mu\text{m}$, $V_{DS}=0.9 \text{ V}$

Table 2 Characteristics of FD-CMOS OP-AMP at 4 K

	design	measurement	
temperature	4 K	4–300 K*	excellent
open loop gain	> 1000	7000	excellent
Output swing	> 1V	1.3 V	excellent
input referred noise	14-20 $\mu\text{V}/\sqrt{\text{Hz}}$	19 $\mu\text{V}/\sqrt{\text{Hz}}$	good
power	1.1 μW	1.3 μW	good
input offset	0 mV	2 mV	good

*: adjustment of bias voltage is required in room temperature operation.

3 Discussions

In case of the next generation space FIR telescope with the next generation FIR detector, the thermal radiation from the telescope and the dark current of the detector should be less than the natural background which consists of zodiacal light, galactic cirrus emission and the cosmic infrared background. In order to achieve background limited observations, the ROIC must have less leakage current compared with the photo-current and less noise compared with the shot noise of the photo-current produced by the natural background in each pixel.

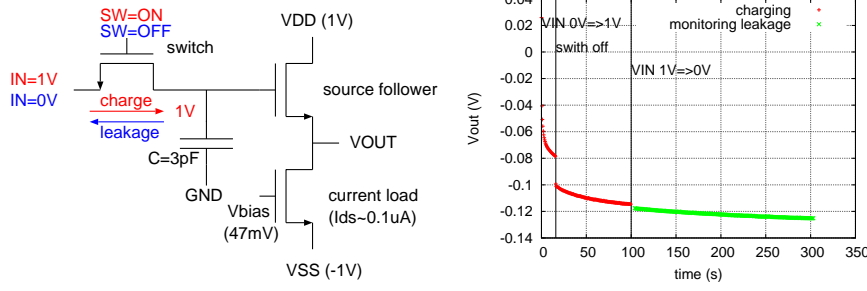


Fig. 5 (Color online) Test circuit for leakage current measurement (left) and the output trend (right). The capacitor (3 pF) is first charged up to the input level (1 V) by switch-on. After switch-off, the input level is shifted to 0 V. The leakage current of the switch FET shifts the voltage at the capacitor node. The shift of the voltage is observed through the source follower. The source follower gain is 0.94 ± 0.01 . The leakage current and off-resistance is estimated to be 1.2×10^{-16} A and $7.5 \times 10^{15} \Omega$ from the voltage trend at 150-240 second.

Table 3 Background signal for a cryogenic space telescope with Nyquist sampling pixel scale

wavelength μm	sky brightness* MJy/str	sky signal [†] e/s/pixel	pixel scale [‡] arcsec
2.2	0.11	2.4e-02	0.076
25	18	5.0e+02	0.86
100	2.5	1.1e+03	3.4
240	1.8	4.6e+03	8.2

*: DIRBE/COBE dark sky¹⁴.

[†]: adopting a spectral resolution $R = 10$ and a total efficiency $\eta = 0.15$.

[‡]: a pixel scale at each wavelength band for a telescope diameter of 3.0 m.

The number of the background photons in each pixel per sec is calculated as follows.

$$N_{\lambda,BG,pix} = I_{\lambda,BG} \Omega_{pix} A_{tel} \frac{1}{E_{photon}} \eta d\lambda = I_{\nu,BG} \frac{\lambda^2 \pi \eta}{16 h R}, \quad (1)$$

where $I_{\nu,BG}$ is the sky brightness and $I_{\lambda,BG} = I_{\nu,BG} d\nu/d\lambda = I_{\nu,BG} c/\lambda^2$, Ω_{pix} is the solid angle of a pixel, $d\lambda = \lambda/R$ is the band width at the spectral resolution of R , $A_{tel} = \pi(D/2)^2$ is the effective area of the telescope (diameter of D), $E_{photon} = hc/\lambda$ is the photon energy, and η is the total quantum efficiency including the optics and the detector. The solid angle of a pixel can be written as $\Omega_{pix} = (\lambda/2D)^2$ if the pixel samples the telescope's point spread function (PSF) in proper Nyquist condition. Table 3 shows the number of the natural background signal in unit of electron per pixel per sec adopting the measurement of the natural background by DIRBE/COBE¹⁴, the spectral resolution $R = 10$, and the optical/detector efficiently $\eta = 0.15$.

In the FIR wavelength regions, order of 1000 electron/sec (0.16 fA) natural background signal is expected. The leakage current of the ROIC must be less than this natural background signal and the measured leakage current of the switch FET is comparable to (with applied voltage of 1.2 V) or ten times smaller than

(with 0.12 V) that of the natural background signal assuming the off-resistance of $7.5 \times 10^{15} \Omega$ measured with 0.9 V.

The ROIC must also have less noise compared with the shot noise produced by the natural background. The natural background signal (0.16 fA) generates a white shot noise of $I_n = \sqrt{2qI} = 7.8 \times 10^{-18} \text{ A}/\sqrt{\text{Hz}}$. This corresponds to voltage noise density of $V_n = I_n/(2\pi fC_i)$ at the output. Adopting the integration capacitance (figure 1) of $C_i = 0.1$ pF and the integration in the 0.1 Hz to 2 Hz bandwidth, this corresponds to 36 μV RMS at the output. Integration of 1/f noise of the OP-AMP (19 $\mu\text{V}/\sqrt{\text{Hz}}$ at 1 Hz) across the same bandwidth leads to 33 μV . Considering the detector capacitance ($C_d = 59$ fF for a germanium BIB detector with a pixel size of $100 \times 100 \mu\text{m}^2$ and thickness of 20 μm in depletion layer and that of 4 μm in blocking layer, adopting a relative permittivity of 16 for germanium), the output noise is a factor of $(1 + C_d/C_i)$ larger than the OP-AMP itself and results in 53 μV RMS at the output. A factor of 1.47 improvement in noise (to use MOSFETs with 2.16 times larger gate width; $W=10.8 \mu\text{m}$, for example) is necessary to achieve natural background limited performance.

Dynamic range is also important because the standard star in the far-infrared astronomy is quite bright (a few Jy, $\text{Jy}=1.0^{-26} \text{ W}/\text{m}^2/\text{Hz}$) compared with the faint target (a few μJy) of the next generation FIR space observatories (such as high-redshift primeval galaxies). The output swing (1.3 V) and the system noise (53 μV) give an order of 10^4 in dynamic range and this is sufficient if we use appropriate secondary standard stars.

Input offset voltage (2 mV) is negligible compared with bias voltage of Ge:Ga FIR photo-conductor (or BIB detector). However, the variation of the offset voltage may affect the uniformity of photo-response among the pixels in case of direct hybrid sensors¹⁵, in which the ROIC has pixel-to-pixel connection to a monolithic detector array. Further investigation of the variation is required.

The power (1.3 $\mu\text{W}/\text{pixel}$) is acceptable for the next generation 32x32 pixels class FIR imaging sensor. We may need further optimization in parameters (W/L for each MOSFETs) for a 64x64 pixel sensor.

4 Conclusions

We have investigated the cryogenic characteristics of FD-SOI CMOS FETs and OP-AMP. We have found that both p- and n-channel FET have good characteristics at the LHT if they have source tie structure. We have confirmed that the characteristics are reproduced in multiple productions. The OP-AMP also shows good characteristics at the LHT. FD-SOI-CMOS has been proven to be an appropriate process for the ROIC of the next generation far-infrared imaging sensors.

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